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Individual charge traps in silicon nanowires

Measurements of location, spin and occupation number by Coulomb blockade spectroscopy

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Abstract. We study anomalies in the Coulomb blockade spectrum of a quantum dot formed in a silicon nanowire. These anomalies are attributed to electrostatic interaction with charge traps in the device. A simple model reproduces these anomalies accurately and we show how the capacitance matrices of the traps can be obtained from the shape of the anomalies. From these capacitance matrices we deduce that the traps are located near or inside the wire. Based on the occurrence of the anomalies in wires with different doping levels we infer that most of the traps are arsenic dopant states. In some cases the anomalies are accompanied by a random telegraph signal which allows time resolved monitoring of the occupation of the trap. The spin of the trap states is determined via the Zeeman shift.

PACS. 73.23.Hk Coulomb blockade; single-electron tunneling – 73.20.Hb Impurity and defect levels; energy states of adsorbed species – 75.75.+a Magnetic properties of nanostructures

1 Introduction

Single electron charges or spins are very appealing as logic bits, either as ultimate classical bits or quantum bits if coherence is used [1–4]. To read such bits, either quantum point contacts or single electron transistors (SETs) are used. SETs have indeed been used as very sensitive electrometers for the (time-averaged) charge on a second quantum dot for over a decade now [5,6]. More recently SETs were used to monitor the time-resolved charge on the second dot or to measure a current by electron counting [7–10]. These experiments allow to measure extremely low currents and to address its full counting statistics [11].

Such experiments are difficult because any device that involves detection of few or single electron charges is subject to the dynamics of surrounding charge traps [12]. This is particularly critical for metallic SETs [13]. For SETs based on the very mature silicon CMOS technology the control of this offset charges seems to be better [14].

These charge traps can be seen as quantum dots whose presence or properties are not controlled. Typically they consist of defects on atomic scale. Therefore their sizes are much smaller than those of dots defined by lithography. If their positions, although being random, can be limited to some region of space, the charge traps are not necessarily a nuisance but can useful. An example are flash memories where the trend is to replace the lithographic floating gate by grown silicon nanocrystals inside the gate oxide. These intentional charge traps have all the same distance from channel and gate electrode and thus the same dynamics [15,16]. Another example are dopants in semiconductors. Efforts are made to control their individual position in a silicon crystal [17]. Indeed, besides the location, their properties are very uniform and solid state quantum bits based on dopants in a silicon crystal — individually addressed by gates and contacts — were proposed as solid state quantum bits [1,2,18]. Silicon is interesting as host material because the spin relaxation time can be very long [19] compared to GaAs. The detection of spins of individual traps in a silicon field effect transistor has recently been reported using random telegraph noise [20,21]. However, in this experiment the traps seem to be in the oxide rather than in the silicon.

In this work, we use nanowire-based silicon transistors operated as SETs at low temperature to detect the location, spin and occupation number of individual charge traps. The excellent quality of the silicon-oxide interface and the precise control of the doping level are the major benefits of silicon technology. This will allow us to attribute the traps to As dopant states. Their capacitive coupling to the SET induces anomalies in the otherwise very regular periodic oscillations of the drain-source conductance G versus gate voltage V_g. We compare the data with simulations obtained after solving the master equation for the network formed by the main dot and the charge trap.

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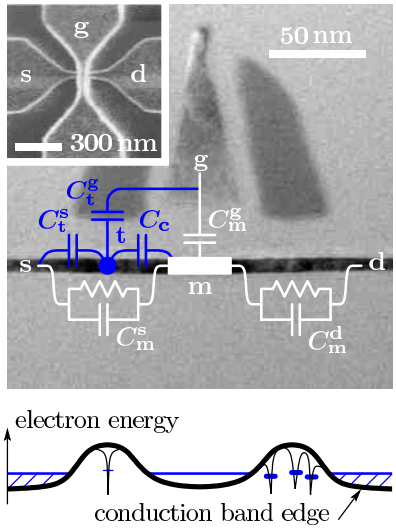

Fig. 1. Sample layout and electrical model. The insert shows a top view after gate electrode etching (no spacers) obtained in a scanning electron microscope. The main image shows a transmission electron micrograph (TEM) of a type B sample along the silicon nanowire (black). The wire shown here is thinner than in the samples used for measurements. Light gray regions are silicon oxide. The darker region in the center is the polysilicon gate with Si_3N_4 spacers on both sides of it. Below, a schematic energy diagram is drawn. The reduced doping level below the spacers and the gate electrode creates a potential barrier, in the middle of which a well is created by a positive gate voltage [23]. Conductance through the barriers separating the well from source and drain occurs by tunneling through a chain of well connected dopants (schematically illustrated in the right barrier) [24]. In more isolated dopants (left barrier) the number of charges is quantized. Such traps are the main concern of this paper. Their interaction with the quantum well is mainly electrostatic. We describe it with the lumped network superimposed to the TEM.

Not only the static time-averaged current is captured by the analysis but also the switching noise which appears near the degeneracy point in gate voltage where the trap occupation number fluctuates.

Finally, a magnetic field was applied in order to probe the spin polarization of the traps via their Zeeman shifts. As expected from simple considerations [22], we observed a majority of singly occupied traps.

2 Samples and set-up

Samples are produced on 200 mm silicon on insulator (SOI) wafers with 400 nm buried oxide and a boron substrate doping of $10^{15}\,\mathrm{cm}^{-3}$. The SOI film is locally thinned down to approximately 20 nm and a 30 nm wide and 200 nm long nanowire is etched from it. A 40 nm long polysilicon control gate is deposited in the middle of the wire (see Fig. 1). There are two types of samples: type A samples with high doping level and type B samples with low doping in the active regions. These different doping levels necessitate slightly different fabrication processes. Type A: the wires are uniformly doped with As, above $10^{19}\,\mathrm{cm}^{-3}$. The gate oxide is only 4 nm thick to allow for good gate control despite the high doping level. Type B: the wires are first uniformly doped at a lower level (As, $10^{18}\,\mathrm{cm}^{-3}$), then, after deposition of the gate electrode and 50 nm-wide Si_3N_4 spacers on both sides of it, a second implantation process increases the doping to approximately $4\times10^{19}\,\mathrm{cm}^{-3}$ in the uncovered regions while the doping level stays low near the gate. In this layout the gate oxide is 10 or 24 nm thick, with a 2 or 4 nm thermal oxide and 8 or 20 nm deposited oxide. Most measurements are made on type B samples, and we use type A samples mainly for comparison.

The measurements were performed in a dilution refrigerator with an electronic base temperature of approximately 150 mK. We used a standard 2-wire low frequency lock-in technique with low enough voltage excitation to stay in the linear regime and a room temperature current amplifier (gain 100 MΩ). For time resolved measurements a DC bias voltage was applied and current measured with a 50 MΩ current amplifier (bandwidth 10 kHz) followed by a 33 kHz AD conversion. For spin sensitive measurements a superconducting magnet was used to apply an in-plane magnetic field up to 16 T.

3 Data

Figure 2 shows typical $G(V_g)$ plots. At room temperature our samples behave as classical (albeit not optimized) n-channel MOSFETs. Below approximately 20 K they turn into single-electron transistors with regularly spaced Coulomb blockade resonances [23]. The period $V_+ = e/C^g$ of these oscillations (e is the absolute value of the electron charge) is determined by the gate capacitance C^g, which in turn can be estimated from the gate/wire overlap and the gate oxide thickness. For the sample with 4 nm (A), 10 nm (B), 24 nm (B) gate oxide the peak spacing is respectively 14 mV ± 4 mV, 10.3 mV ± 0.5 mV, 15.3 mV ± 0.8 mV. This corresponds to a gate capacitance of 11 aF, 15.5 aF, 10.5 aF. For type A samples the gate capacitance is in good agreement with the simple planar capacitance estimation. For type B samples where the gate oxide thickness is of the same order as the dimensions of the wire, the 3-dimensional geometry has to be taken into account. The gate capacitance of the type B samples is increased with respect to the type A samples because the flanks of the wire play a more important role. A 3-dimensional numerical solution obtains a good agreement with the measured capacitances [23].

The single particle level spacing is less than 0.2 meV, much smaller than the charging energy and comparable to kT. The peak spacing statistics has already been measured and compared to theory [25]. Here we focus on anomalous regions where the conductance contrast is markedly reduced and a phase shift of the Coulomb blockade oscillations occurs. They cause tails in the Gaussian peak-spacing distribution. Such perturbations to the periodic pattern are marked with circles in Figure 2. In the type B samples with low doping, these perturbations occur only

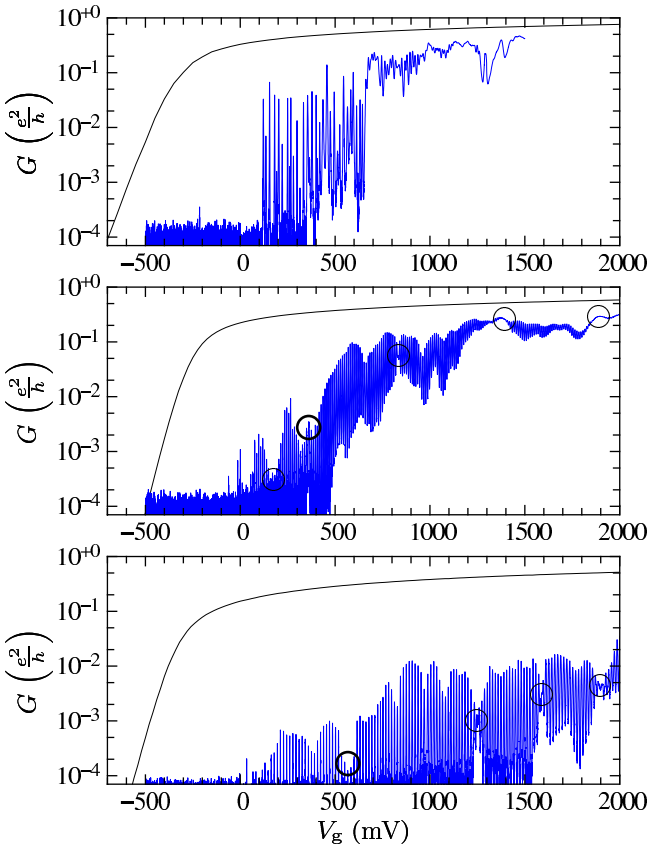

Fig. 2. Drain-source conductance versus gate voltage for 3 different samples. All samples have the same width and gate length but the sample in the upper panel is of type A with a 4 nm gate oxide, while the samples in the lower panels are of type B, the gate oxide being 10 nm in the middle panel and 24 nm in the lower panel. The smooth field-effect characteristics at room temperature (black lines) are replaced by Coulomb blockade oscillations at base temperature (blue curves). The period is determined by the surface area of the nanowire/gate overlap. The Coulomb blockade oscillations in the upper panel are irregular compared to the ones in the lower panels where only a few anomalies perturb the otherwise very regular spectrum. These anomalous regions with reduced contrast and fluctuating peak spacing are highlighted with circles. The anomalies marked with bold circles are studied in detail in this work.

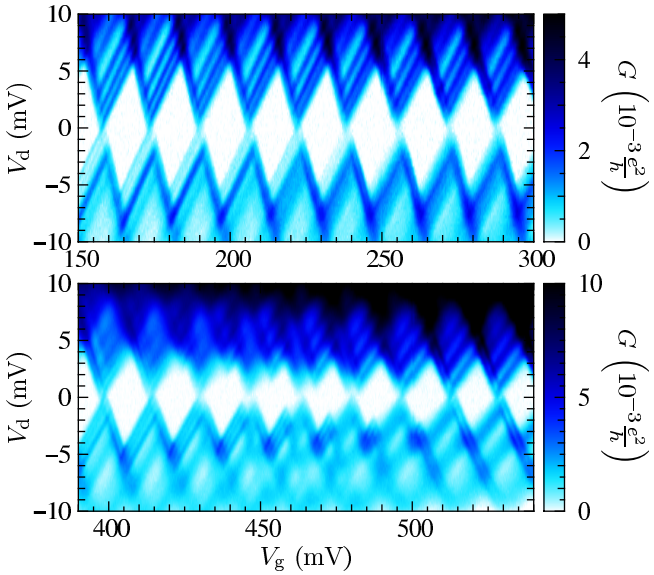

Fig. 3. 2D-plots of the measured drain-source conductance versus gate and drain voltages in an unperturbed, very periodic gate voltage range (upper panel), and in an anomalous region where a charge trap is observed (lower panel). White areas correspond to Coulomb blockaded regions (no detectable current). The lines inside the conducting regions do not correspond to the excited states of the dot: the quantum dot is diffusive and the mean single-particle level spacing is much lower than the observed spacing inside the diamonds [25]. In addition, the lines are identical in a long sequence of diamonds, which should not be the case for excited states. Thus we rather attribute these lines to additional conduction channels in the drain barrier opening at higher bias (chains of well connected dopants lying somewhat higher in energy than the drain Fermi level). Compared to the lower panel of Figure 2, the anomalous region has shifted by 50 mV in gate voltage after thermal cycling between base and room temperature. We do not observe such shifts as long as the sample is kept cold.

rarely (we observe typically 3 to 5 per sample). In the unperturbed regions, the height of the Coulomb blockade peaks shows long-range correlations. In the type A samples with high doping level the perturbations are more frequent and as a result the whole spectrum looks irregular (see top panel of Fig. 2). This suggests that the perturbations are related to the doping.

In the measured stability diagram, i.e. the 2D plot of conductance versus gate and bias voltages, the perturbations are even more visible (see Fig. 3). In the perturbed regions additional teeth appear in the Coulomb diamonds.

We develop a simple model based on a trap state located in the vicinity of the quantum dot, and compare the simulation with the experimental data.

4 Model

The quantum dot formed by the gate electrode in the middle of the wire is separated from the source and drain reservoirs by a piece of silicon wire containing only a few tens (type B) or hundreds (type A) of dopants. In the type A samples these access regions extend from the border of the gate electrode to the regions where the wire widens (see Fig. 1) and its resistance becomes negligible. In the type B samples only the parts of the wire below the spacers contribute significantly to the access resistance and the highly doped parts of the wire can be considered as part of the reservoirs.

Electrons pass through these access regions by transport via the dopant states[1]. As the dopants are distributed randomly and the coupling between them depends exponentially on their distance, the strength of this coupling is distributed over a wide range. Therefore transport takes

[1] Direct tunneling through a 50 nm thick barrier leads to access resistances much higher than observed, even for barrier heights of a few meV.

place mainly through a percolation path formed by well connected dopants [22] while other dopant states are only weakly connected and their occupation is a good quantum number (see Fig. 1). We attribute the anomalies in the Coulomb blockade spectrum to the electrostatic interaction of the quantum dot with such a charge trap formed by an isolated dopant site.

We model this with the lumped network shown in Figure 1. Similar models have been considered in references [26] and [27]. A small trap (t) is capacitively coupled to source (s), drain (d), gate (g) and to the main dot (m). We note $C_i = C_i^{\mathrm{s}} + C_i^{\mathrm{d}} + C_i^{\mathrm{g}}$ and $X_i = C_i^{\mathrm{s}} V_{\mathrm{s}} + C_i^{\mathrm{d}} V_{\mathrm{d}} + C_i^{\mathrm{g}} V_{\mathrm{g}}$ ($i = \mathrm{m}, \mathrm{t}$). After some calculation, the electrostatic energy of the two dot system can be expressed as a function of the charges Q_{m} on the main dot and and Q_{t} in the trap.

$$W(Q_{\mathrm{m}}, Q_{\mathrm{t}}) = \underbrace{\frac{(Q_{\mathrm{m}} + \beta_{\mathrm{t}} Q_{\mathrm{t}} + X)^2}{2C}}_{M(Q_{\mathrm{m}}, Q_{\mathrm{t}})} + \underbrace{\frac{(Q_{\mathrm{t}} + X_{\mathrm{t}})^2}{2\,(C_{\mathrm{t}} + C_{\mathrm{c}})}}_{T(Q_{\mathrm{t}})} \qquad (1)$$

where C_{c} is the capacitive coupling between dot and trap, $\beta_{\mathrm{t}} = \frac{C_{\mathrm{c}}}{C_{\mathrm{t}} + C_{\mathrm{c}}}$, $C = C_{\mathrm{m}} + \beta_{\mathrm{t}} C_{\mathrm{t}}$ and $X = X_{\mathrm{m}} + \beta_{\mathrm{t}} X_{\mathrm{t}}$. For a small trap ($C_{\mathrm{m}} \gg C_{\mathrm{t}}$) these renormalizations are weak: $C \approx C_{\mathrm{m}}$ and $X \approx X_{\mathrm{m}}$. Note that the expression for W is symmetric under exchange of main dot and trap. Expressions M and T have different forms because we attributed the interaction term entirely to M to ease further analysis. W is plotted in the top panel of Figure 4.

We focus on the structure of the Coulomb blockade conductance fixed by equation (1) and not on the exact value on the conductance plateaus. Therefore we choose as simple as possible the following parameters which are necessary for the simulation but do not affect the structure of the conductance diagram.

We suppose all transmission coefficients to be constant, the ones connecting the main dot to source and drain being 1000 times higher than the ones connecting the trap to the main dot and source or drain. Therefore electrons can be added or removed from the trap, but their contribution to the total current through the device is negligible. This contrasts with models of stochastic Coulomb blockade [28] or in-series quantum dots [29,30] where the current has to pass through both dots.

In terms of kinetic energy, we describe the main dot as metallic (negligible single-particle level spacing Δ, i.e. $\Delta \ll kT$) and we consider only one non-degenerate energy level for the trap. Its energy can be accounted for through a gate-voltage offset in the parameter X_{t}. This parameter also allows to correct for the unphysical electrostatic self-energy when one electron is in the trap. In the presented simulations we only compensate the self energy but do not add a kinetic energy. In source and drain we suppose a uniform density of states. We assume fast relaxation of kinetic energy inside the dot and the reservoirs, i.e. thermal distributions in the electrodes and the main dot, even for nonzero bias voltage. With these assumptions, the transition rates of an electron in the main dot to the source or drain reservoirs or from the reservoirs to the dot are proportional to the auto-convolution of the Fermi function. The transition rates from or towards the trap are directly proportional to the Fermi function [31].

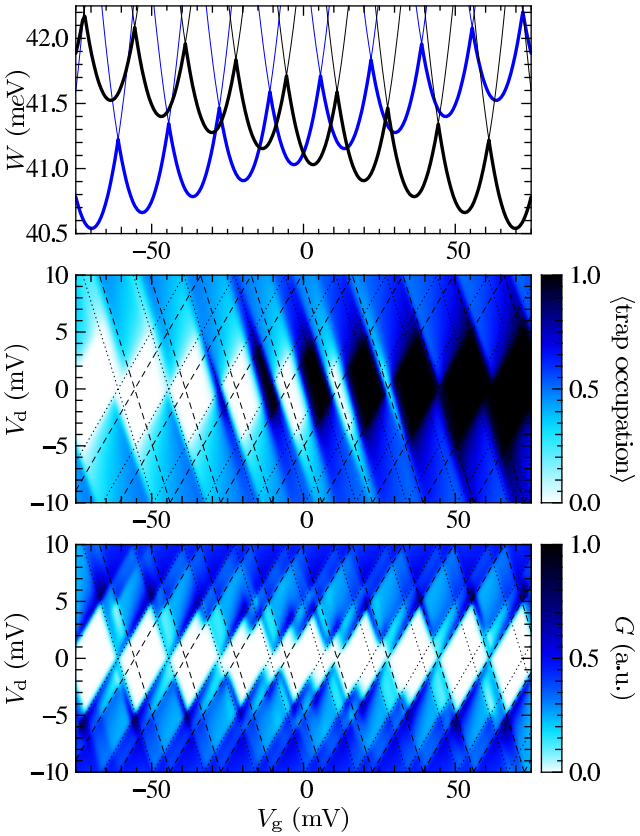

Fig. 4. Numerical study of a trap coupled to the source and to the main quantum dot, as sketched in Figure 1. Parameters: effective temperature: $T = 1\,\mathrm{K}$; main dot: $C_{\mathrm{m}}^{\mathrm{g}} = 10\,\mathrm{aF}$, $C_{\mathrm{m}}^{\mathrm{d}} = C_{\mathrm{m}}^{\mathrm{s}} = 11\,\mathrm{aF}$; trap: $C_{\mathrm{t}}^{\mathrm{g}} = 0.007\,\mathrm{aF}$, $C_{\mathrm{t}}^{\mathrm{s}} = 0.3\,\mathrm{aF}$, $C_{\mathrm{t}}^{\mathrm{d}} = 0$, $C_{\mathrm{c}} = 0.15\,\mathrm{aF}$. The trap can either be empty or charged with one electron. The upper panel shows the energy for the different charge states at zero bias in function of gate voltage. The blue parabolas are for empty trap, the black ones for occupied trap. The thick blue and black lines indicate the ground state of the main dot for respectively empty and occupied trap. The middle panel shows the self-consistent mean occupation number of the trap, the lower panel the resulting conductance through the dot. The effect of the charge trap is to shift the Coulomb blockade diamonds of the main dot depending on the charge in the trap. The dotted (dashed) lines indicate the position of the diamonds when the trap is empty (occupied). This result is in very good agreement with the experimental data shown in the lower panel of Figure 3.

The statistical probability for each state $(Q_{\mathrm{m}}, Q_{\mathrm{t}})$ of the system can now be calculated by solving the master equation numerically and gives access to the mean current through the system.

Results of such a numerical study are presented in Figure 4. The middle panel shows the mean occupation of the trap. On a large scale, the trap becomes occupied with increasing gate voltage. In the central region of the figure however, whenever an electron is added onto the main dot, the electron in the trap is repelled and only later it is reattracted by the gate electrode. Inversely, the trap charge

repels the charges on the main dot and the Coulomb blockade structure of the main dot is shifted to higher gate voltage when the trap is occupied (see lower panel). The two Coulomb blockade structures for unoccupied and occupied trap are respectively indicated by dotted and dashed lines in the middle and lower panel of Figure 4.

This explanation is illustrated in terms of energy in the top panel of Figure 4, which shows the energies for the different charge configurations. The crossings of the blue (black) parabolas give the positions of the Coulomb blockade peaks for empty (occupied) trap. The shift between the crossings of the black parabolas with respect to the crossings of the blue parabolas and the shift of the dashed lines with respect to the dotted lines are due to the term $\beta_\mathrm{t} Q_\mathrm{t}$ in $M(Q_\mathrm{m}, Q_\mathrm{t})$. Knowing that one Coulomb blockade oscillation corresponds to a change of e in $\beta_\mathrm{t} Q_\mathrm{t} + X$, the shift due to $\Delta Q_\mathrm{t} = e$ is

$$\delta V_\mathrm{g} = \beta_\mathrm{t} V_+ \tag{2}$$

where V_+ is the Coulomb blockade peak spacing of the main dot.

We will now determine the width of the anomaly in the Coulomb blockade spectrum at low bias voltage. It is given by the gate voltage range where the occupation of the trap oscillates at zero bias. In the top panel of Figure 4 this is the zone between the first and the last crossing of the thick black line and the thick blue line. First we calculate ΔM, the difference of the ground state energies for empty and occupied trap arising from the term M in equation (1). Then we calculate the change in gate voltage necessary for $T(-e) - T(0)$ to exceed this difference.

ΔM reaches its extreme values when, for one state of the trap, the main dot is at a degeneracy point (the kinks in the thick lines), where $M = \frac{(e/2)^2}{2C}$. For the other state of the trap, the main dot is then a fraction β_t of a Coulomb blockade period away from the degeneracy point and $M = \frac{e^2(1/2-\beta_\mathrm{t})^2}{2C}$. The extrema of ΔM are therefore $\pm\frac{e^2}{2C}\beta_\mathrm{t}(1-\beta_\mathrm{t})$.

The gate voltage dependence of term T is given by $\alpha_\mathrm{t} = \frac{1}{-e}\frac{d}{dV_\mathrm{g}}\left(T(-e) - T(0)\right) = \frac{C_\mathrm{t}^\mathrm{g}}{C_\mathrm{t}+C_\mathrm{c}}$. Note that α_t is the long-range gate voltage lever arm of the trap over several Coulomb blockade oscillations, where the charge of the main dot has to be considered as relaxed with the source and drain Fermi levels. $T(-e) - T(0)$ has to change from $+\frac{e^2}{2C}\beta_\mathrm{t}(1-\beta_\mathrm{t})$ to $-\frac{e^2}{2C}\beta_\mathrm{t}(1-\beta_\mathrm{t})$ in order to toggle the trap definitively. Therefore the width ΔV_g of the anomaly is given by $e\alpha_\mathrm{t}\Delta V_\mathrm{g} = 2\frac{e^2}{2C}\beta_\mathrm{t}(1-\beta_\mathrm{t})$ or

$$\Delta V_\mathrm{g} = \frac{\beta_\mathrm{t}(1-\beta_\mathrm{t})}{\alpha_\mathrm{t}}\alpha_\mathrm{m} V_+ \tag{3}$$

where $\alpha_\mathrm{m} = \frac{C^\mathrm{g}}{C}$ with $C^\mathrm{g} = C_\mathrm{m}^\mathrm{g} + \beta_\mathrm{t} C_\mathrm{t}^\mathrm{g}$ is the gate-voltage lever arm of the main dot.

We have identified $\alpha_\mathrm{t} = \frac{C_\mathrm{t}^\mathrm{g}}{C_\mathrm{t}+C_\mathrm{c}}$ and $\beta_\mathrm{t} = \frac{C_\mathrm{c}}{C_\mathrm{t}+C_\mathrm{c}}$ as parameters determining the structure of the trap signature. Both do not depend on the absolute value of the trap's capacitances. Indeed, if one allows only 0 or 1 electron in the trap, the absolute value of the trap capacitances enters the problem only indirectly by slightly modifying the capacitance matrix of the main dot and, in the limit of a small trap, does not enter the problem at all. Therefore, our model only contains 2 effective parameters for the trap instead of 3 (C_t^g, C_t^s, C_c). All 3 parameters are only significant if the trap can accommodate 2 or more electrons. In this case the spacing between the anomalies gives access to the absolute values of the trap capacitances.

So far we have considered traps on the source side of the dot. We will now describe how the signature depends on the position of the trap with respect to the dot. If as in the example of Figure 4 the trap is on the source side, the zones of empty and occupied trap in the $(V_\mathrm{g}, V_\mathrm{d})$ plane are aligned with the negative slope of the diamonds (see middle panel of Fig. 4). This is due to the fact that along a line parallel to the negative slope of the diamonds the highest occupied level in the dot stays at constant energy with respect to the source Fermi level. As the trap is controlled mainly by source and dot, its occupation stays constant in this direction. The weak influence of the gate electrode on the trap causes small deviations from this direction. This can be seen in the middle panel Figure 4b: the limits separating white (empty) and black (occupied) zones are not exactly parallel to the diamond slopes. Due to this almost perfect alignment, changes in the occupation number of the trap occur only at the positive slopes of the diamonds. They cause the characteristic teeth of constant width δV_g to appear on the positive slope of the diamonds. In the same way, the teeth appear on the negative slope if the trap is on the drain side of the dot.

As a summary, Figure 5 illustrates the relation between the trap's capacitance matrix and its signature. If the teeth of constant width are visible at the positive slope of the Coulomb blockade diamonds, the trap is on the source side of the dot. If they are visible at the negative slope, the trap is on the drain side. The width of the teeth depends on β_t, the width of the anomalous region essentially on α_t (for β_t close to $\frac{1}{2}$, where the anomalies are well visible).

5 Position and nature of the traps

As an illustration, from the lower panel of Figure 3 we infer $\alpha_\mathrm{t} \approx 0.015$ and $\beta_\mathrm{t} \approx 0.3$. These are the actual parameters that have been chosen for the simulation in Figure 4 and the lower panels of Figures 3 and 4 are indeed very similar. As for all impurities we observed, α_t is small. This is what we expect for a trap inside the silicon wire. The coupling to the gate electrode is much weaker than the coupling to the main dot or the source electrode because the dielectric constant of the oxide barrier ($\epsilon_{\mathrm{SiO}_2} = 4$) is much smaller than that of bare silicon ($\epsilon_\mathrm{Si} = 12$), which, in addition, is enhanced near the insulator–metal transition [32].

Traps located outside the wire can be ruled out. Traps located deep inside the oxide can be excluded because their transmissions would be too weak to observe statistical mixing of occupied and unoccupied trap states during our acquisition time below 1 s. Similar devices including

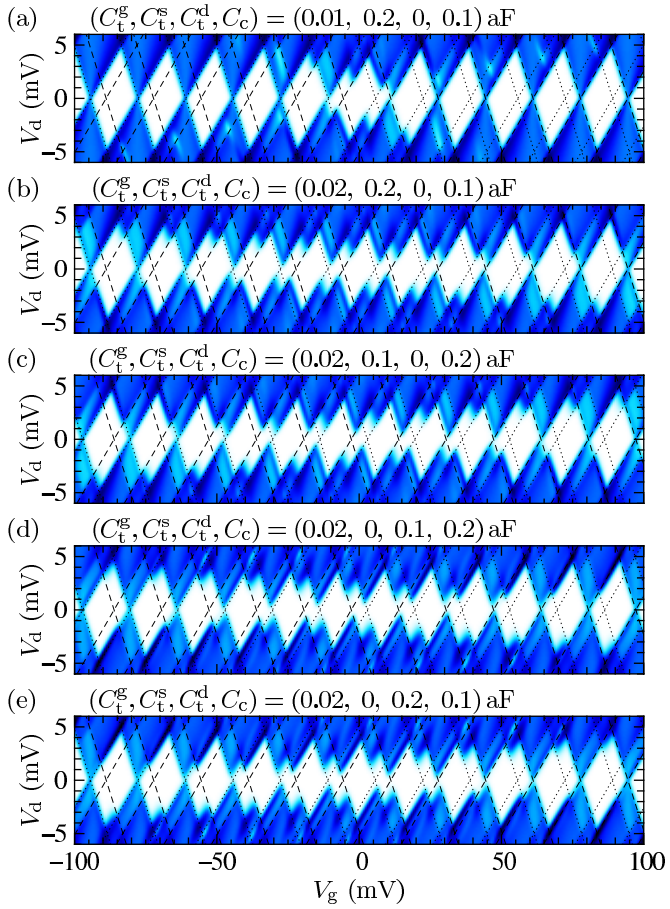

Fig. 5. Calculated trap signatures for different sets of parameters. (a) The trap is close to the source. (b) The coupling to the gate electrode is reduced by a factor of 5. The signature becomes wider. (c) The coupling to the source is reduced, the coupling to the dot increased. (d) The trap is placed on the drain side of the dot instead of the source side. (e) The coupling to the dot is reduced, the coupling to the drain increased.

intentional silicon nanocrystals at the interface between thermal oxide and deposited oxide have been studied in views of memory applications [16,33]. The measured lifetime of charges in the nanocrystals exceeds 1 s by orders of magnitude already at room temperature and at low temperature gate voltages of approximately 5 V have to be applied in order to toggle the charge in the nanocrystals. Therefore the traps must be inside the Si wire or at its interface with the oxide. But the interface traps are unlikely. The used technology attains less than $10^{11}\,\mathrm{cm}^{-2}$, corresponding to a few units per sample. As they are distributed throughout the entire band gap it is very unlikely to observe several of them in the small energy window $\alpha_t(V_g^{\max} - V_g^{\min}) \approx 30\,\mathrm{meV}$ that we scan in our measurement. The most likely traps are therefore defects in the silicon wire or As donor states. Given the volume of the access regions under the spacers and the doping level N_D, there are approximately 70 donor states under the spacers in devices of type B. We estimate the width of the impurity band to be $\frac{e^2}{\epsilon_0 \epsilon_r N_D^{-1/3}} \approx 150\,\mathrm{meV}$ [22]. One should therefore expect around 15 dopants in the energy window. Typically we record 3 to 5 anomalies. Indeed we do not expect to observe anomalies for all dopants because the charge on well connected dopant sites is not quantized and, according to our model, dopants very close to the dot ($\beta_t \approx 1$) or to the reservoir ($\beta_t \approx 0$) cause very small anomalies.

In the type A samples the doping level in the access regions is more than 10 times higher than in the type B samples. The whole Coulomb blockade spectrum should therefore be anomalous. Indeed, the spectrum is much less regular (see Fig. 2) than for the type B samples, especially for low gate voltage, but we cannot distinguish signatures as clear as in the type B samples. This is consistent because in the type A samples the mean distance between impurities is less than 3 nm and they are too well connected for the charge on them to be well quantized. In other words, the wire is very close to the insulator–metal transition. Our doping level is in fact already higher than the bulk critical As concentration $N_c = 8.6 \times 10^{18}\ \mathrm{cm}^{-3}$ [34,35].

We have deduced that the observed traps lie inside the wire. The position of the trap along the wire can also be determined. First we can distinguish on which side of the dot the trap is: teeth on positive slope of the diamonds indicate a trap on the source side, teeth on the negative slope a trap on the drain side. Then the parameter β_t gives the ratio between the capacitances towards the main dot and the source (or drain) electrode. As the dielectric constant of the wire is much higher than the surrounding silicon oxide, this ratio can be translated linearly to a position in direction of the wire. In the example of Figure 3 with $\beta_t \approx 0.3$ we would expect the impurity to be located $\frac{2}{3}$ on the way from the dot (edge of the gate electrode) to the source reservoir (source side edge of the spacer).

6 Time-resolved occupation number

In the preceding sections we assumed charge traps with changing mean occupation number to explain anomalies in the mean conductance through a Coulomb blockaded quantum dot. Yet the measurements of the mean current have not allowed us to measure the occupation number of the trap directly. But the currents through the main dot differ for empty and occupied trap because the position of the Coulomb blockade resonances is shifted, and at the anomalies where the mean occupation number of the trap is different from 0 and 1, the fluctuations of the occupation number should create a random telegraph signal (RTS) [36,20,21,37] in the current through the main dot.

Near most of the trap signatures we do not observe increased noise or only a small increase. Only rarely the trap signatures are accompanied with a clear RTS signal. Indeed, charge can be quantized in states with tunneling rates up to the GHz range. Thus, with our measurement in the kHz range we can only observe switching for traps with exceptionally weak coupling while charges in traps with stronger coupling are still sufficiently quantized to produce clear signatures in the mean current.

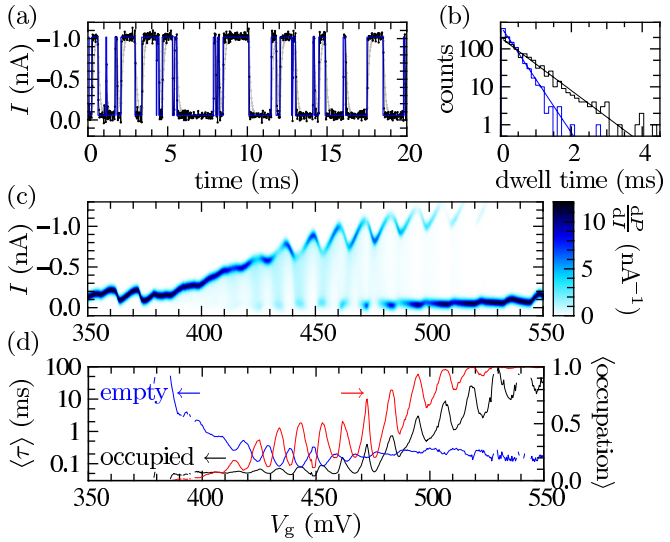

Fig. 6. Analysis of a trap signature with switching. Sample of type B with 24 nm gate oxide. The width of the wire is 80 nm instead of 30 nm. (a) A RTS trace taken at $V_g = 500\,\mathrm{mV}$, $V_d = -6\,\mathrm{mV}$. Light gray trace: raw data. Black trace: data after compensation of the time constant τ_{amp} of the current amplifier ($I' = I + \tau_{amp}\frac{dI}{dt}$). Blue line: fitted signal. The detection time is approximately 30 μs. (b) Histograms of the times spent in the weak current state (occupied trap, black) and the −1 nA state (empty trap, blue). The time constants (averages of these times) are 0.31 ms and 0.62 ms. The corresponding exponential distributions (straight lines) fit well the histograms. (c) Current histogram at $V_d = -6\,\mathrm{mV}$. The nonzero density between the two current levels is due to the finite rise time. The current for unoccupied trap is always higher than for occupied trap. (d) Time constants of the empty and occupied levels in function of gate voltage and occupation number of the trap.

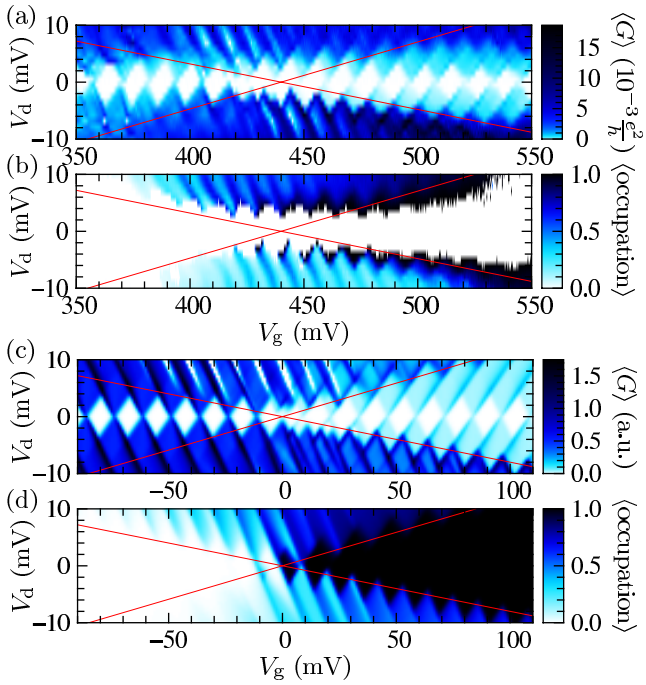

Fig. 7. Comparison of measured occupation number and simulation. Same trap as in Figure 6. (a) Mean differential conductance obtained by numerical derivation of the mean current. (b) Occupation of the trap obtained from the duty cycle of the RTS signal. Regions where no clear RTS could be detected are left white. (c) and (d) Simulation with the following parameters: main dot: $C_m^g = 13\,\mathrm{aF}$, $C_m^s = 10\,\mathrm{aF}$, $C_m^d = 16\,\mathrm{aF}$; trap: $C_t^g = 0.013\,\mathrm{aF}$, $C_t^s = 0.10\,\mathrm{aF}$, $C_t^d = 0$, $C_c = 0.16\,\mathrm{aF}$. In units of the drain-dot barrier transmission, the source-dot barrier transmission is 10 for empty trap and $\frac{1}{10}$ for occupied trap, the source-trap barrier transmission $\frac{1}{1000}$ and the trap-dot barrier transmission $\frac{1}{3000}$.

An example where a clear RTS signal is observed is given in Figure 6a. The distribution of the times spent in the two states follows the exponential distribution expected for a RTS (see Fig. 6b).

The color plot of the current distribution in Figure 6c shows the evolution of the two current levels (the darker regions denote higher current probability) in function of gate voltage. Above 380 mV the two levels are very different. This difference is most likely due to electrostatic interaction of the trap and the current path through the barrier: depending on the state of the trap, the dopants through which the main part of the current flows are well or poorly aligned in energy. The fact that the current levels never cross simplifies greatly the assignment of the high and low current levels to the states of the trap. The high current trace being most likely at low gate voltage and the low current trace being most likely at high gate voltage allows to attribute the high current to empty trap and the low current to occupied trap.

The time constants of the empty and occupied state are plotted in Figure 6d. In accordance with panel (c), the time constant for the empty trap decreases with gate voltage while the time constant for the occupied trap increases. Superimposed with this slow change there are oscillations with a period of 12 mV, the peak spacing of the main dot. The observed time constants are bounded below by the detection time of 30 μs and time constants close to the detection time are overestimated [38]. However, our observation of slow changes and oscillation of the time constants are not affected by this limitation. We concentrate now on the mean occupation number given by $\frac{\tau_{occupied}}{\tau_{occupied}+\tau_{empty}}$. This ratio is unbiased even if the time constants are overestimated [38]. It goes from 0 at low gate voltage to 1 at high gate voltage and strongly oscillates near $V_g = 450\,\mathrm{mV}$ (see Fig. 6d). As explained in Section 4 for the case of low bias, this oscillation is due to the discrete charge on the main dot which cycles the trap several times between empty and occupied state. It is not observed in RTS in larger devices without Coulomb blockade [36]. In Figure 7 the occupation probability for different bias voltages is compared with simulation. As in Figure 4, the oscillations are aligned parallel to the negative slopes of the Coulomb blockade diamonds indicating that the trap is on the source side of the dot.

RTS (i.e. current through the trap) only occurs when the trap is in the bias window. For large gate and bias voltage excursions where the charging energy of the main

dot is negligible, the main dot can be considered as part of the drain reservoir. The zone where the trap is in the bias window is then delimited by slopes $\frac{C_t^g}{C_t}$ and $-\frac{C_t^g}{C_c}$ (indicated by straight lines in Fig. 7), just as for a single quantum dot. These slopes give another more straightforward access to the parameters α_t and β_t. In accordance with the shape of the teeth in panel (a) we get $\alpha_t = 0.05$ and $\beta_t = 0.6$.

The mean occupation of the trap is higher for positive drain voltage than for negative drain voltage, indicating a higher transmission rate of the trap towards source than towards the main dot.

In Figures 7c and 7d we try to reproduce panels (a) and (b). For this simulation we reduce by a factor of 100 the transmission of the source barrier of the main dot when the trap is occupied. This reproduces the lines of reduced differential conductance at positive drain voltage (compare Figs. 7a and 7c). In the simulation the oscillations of the trap occupation decay more rapidly with bias voltage than in the measurement. This could be related to our approximation of a thermal distribution of kinetic energies in the main dot, which is certainly not accurate at high bias voltage.

Charge traps are generally believed to be not only responsible for RTS noise but also for $1/f$ noise in SETs [12] and decoherence [39]. These interpretations imply a large number of traps with small influence on the device (in our model $\beta_t \approx 0$). Such traps could be dopants in the reservoirs or the substrate.

7 Spin

Under magnetic field, via the Zeeman energy, the spin of the trap state leads to a gate voltage shift of the trap signature. It is given by:

$$e\alpha_t \frac{\partial V_g}{\partial B} = g\mu_B \Delta S_z \qquad (4)$$

where μ_B is the Bohr magneton and ΔS_z the change in spin quantum number of the trap state in direction of the magnetic field when an electron is added to the trap. It can take the values $\pm\frac{1}{2}$. If there are already electrons in the trap higher changes are also possible, but they imply spin flips and such processes are expected to be very slow [40]. The Landé factor g for impurities in Si and SiO_2 has been measured in [41]. The observed renormalizations are beyond the precision of our measurements, therefore we take $g = 2$. The gate-voltage lever-arm of the trap states α_t is very weak as we have shown above. The Zeeman shifts should therefore be strong.

Indeed, the magnetic field clearly shifts the trap signature in Figure 8 to lower gate voltage. In order to identify the shift as the Zeeman effect, we compare it quantitatively with the prediction of our model. The shift of the resonances due to the trap is half the peak spacing, thus $\beta_t = \frac{1}{2}$ (see Eq. (2)). The lever arm for the main dot is for this gate voltage $\alpha_m = 0.26$, and the width of the trap signature varies from 2.5 periods at 0 T to 1.5 periods at 16 T. This implies a gate-voltage lever arm for the trap of $\alpha_t = 0.026...0.043$ (see Eq. (3)) which we interpolate as a linear function of magnetic field. The dotted line in Figure 8 is obtained if we put this lever arm and $S_z = -\frac{1}{2}$ in equation (4). It is in very good agreement with the measured shift and confirms our model. The increase of the lever arm with magnetic field could be explained as follows. In the access regions the nanowire is close to the metal-insulator transition and the dopant states strongly increase the dielectric constant [34]. Under magnetic field the localization length could be reduced due to shrinking of orbital states [22] or due to misalignment of dopant states in resonance at zero field. With the localization length the capacitive coupling towards the main dot and the reservoir decreases while the geometric gate capacitance remains unaffected.

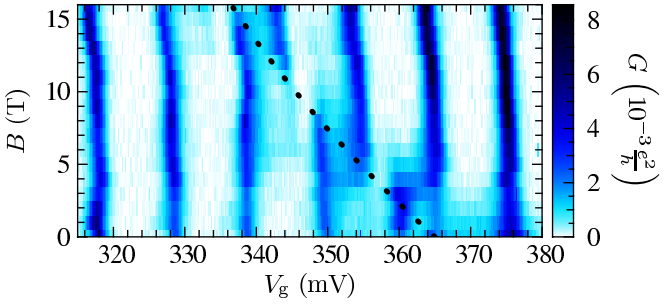

Fig. 8. Shift of a trap signature with magnetic field. The dotted line indicates the Zeeman shift expected for a trap state being occupied by a first electron. It depends on the gate-voltage lever-arm which in turn is determined by the width of the signature. This prediction of the Zeeman shift follows exactly the observed shift.

We observe such Zeeman shifts in the majority of our samples. In most cases the trap signature shifts to lower gate voltage as in Figure 8. This is what we expect for isolated traps occupied with one electron. When a trap state is occupied with a second electron it has to occupy the energetically less favorable state whose energy is increased by the Zeeman effect. This leads to a shift towards higher gate voltage under magnetic field. Although isolated As-donor sites in Si can only be occupied by one[2] electron due to Coulomb repulsion, clusters of two donors could contain two or more electrons [42]. For not too high doping levels however, clusters should be rare. Accordingly we observe much less shifts to higher than to lower gate voltage. In devices based on similar technology Xiao et al. observed that all shifts occurred to higher gate voltage [20,21] indicating doubly occupied traps. With precise measurements of the Landé factor they located the traps inside the oxide. This difference also supports that the traps in our device are not located in the oxide but inside the silicon wire.

[2] Arsenic donors can be populated with 2 electrons but the second electron is so weakly bound that in the scale of our devices it can be considered as delocalized. See for example reference [22].

8 Outlook

Dopant states in silicon could provide very scalable solid state quantum bits, based on charge, electron spin or nuclear spin. But it is still very difficult to control their position individually. On the other hand, with several gate electrodes one could imagine to select suitable dopants out of a large number of randomly distributed dopants. In this context we have presented how the capacitance matrix of charge traps near a small silicon single-electron transistor can be determined and we have shown how the gate-voltage dependence of the occupation is related to the spin of the trap state and that the charge in these traps can be read out. These charge traps are attributed to arsenic dopant states. At a doping level of $10^{18}\,\mathrm{cm}^{-3}$ we observe several well isolated dopant states per device as well as percolation paths of well connected dopants linking the main quantum dot to the reservoirs. In similar geometries with multiple gate electrodes the coupling between the dopants could be tuned by changing their alignment in energy with the well connected dopants. Such randomly distributed dopants are probably more suited for electron spin quantum bits than for charge quantum bits where two dopant sites with small distance are necessary. In this perspective we are working on measurement of the relaxation time of the electron spin in the observed traps. Together with the excellent stability in time as well as its full compatibility with CMOS technology our system could be a good basis for scalable quantum bits.

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